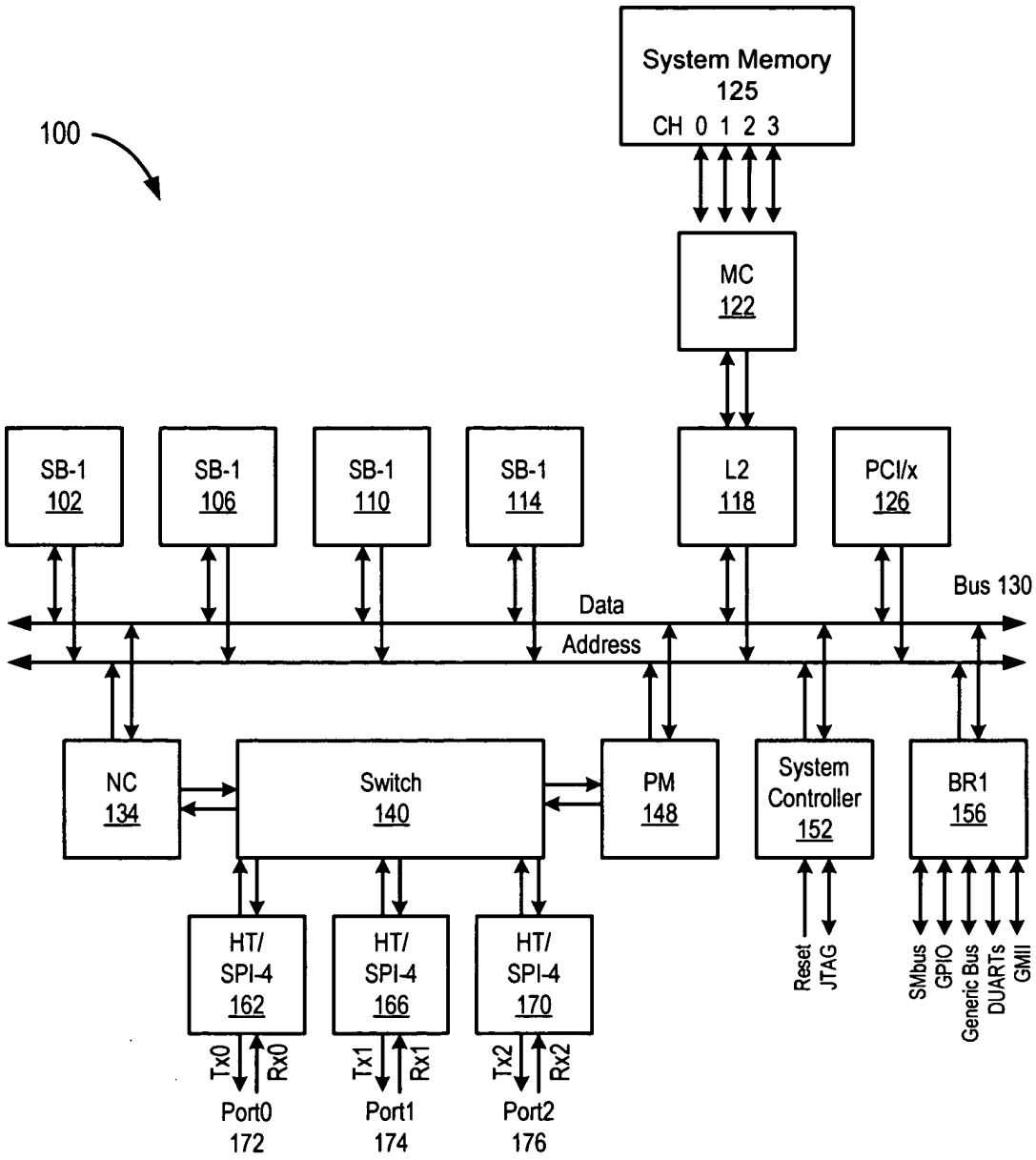

100
System Memory
125
CH 0 1 2 3
MC
122
SB-1
102
SB-1
106
SB-1
110
SB-1
114
L2
118
PCI/x
126
Bus 130
Data
Address
NC
134
Switch
140
PM
148
System
Controller
152
BR1
156
HT/
SPI-4
162
HT/
SPI-4
166
HT/
SPI-4
170
Tx0
Rx0
Tx1
Rx1
Tx2
Rx2
Port0
172
Port1
174
Port2
176
Reset
JTAG
SMbus
GPIO
Generic Bus
DUARTs
GMII

Figure 1

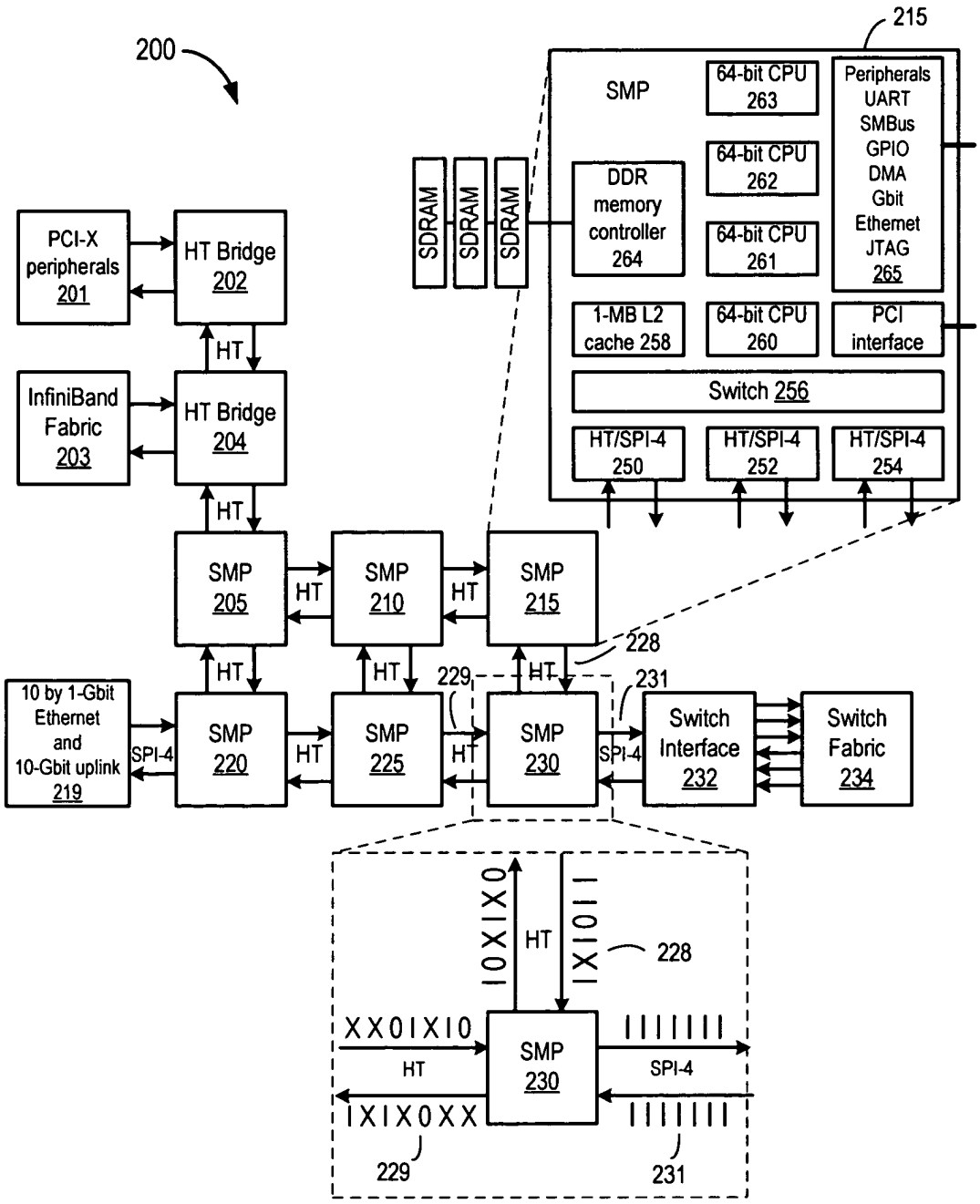

200
215
SMP
64-bit CPU 263
64-bit CPU 262
64-bit CPU 261
64-bit CPU 260
Peripherals UART SMBus GPIO DMA Gbit Ethernet JTAG 265
PCI interface
DDR memory controller 264
SDRAM
SDRAM
SDRAM
1-MB L2 cache 258
Switch 256
HT/SPI-4 250
HT/SPI-4 252
HT/SPI-4 254
PCI-X peripherals 201
HT Bridge 202
InfiniBand Fabric 203
HT Bridge 204
HT
SMP 205
SMP 210
SMP 215
228
229
231
10 by 1-Gbit Ethernet and 10-Gbit uplink 219
SPI-4
SMP 220
SMP 225
SMP 230
Switch Interface 232
Switch Fabric 234
10X1X0
11101X1
XX0IX10
IXIX0XX
SMP 230

Figure 2

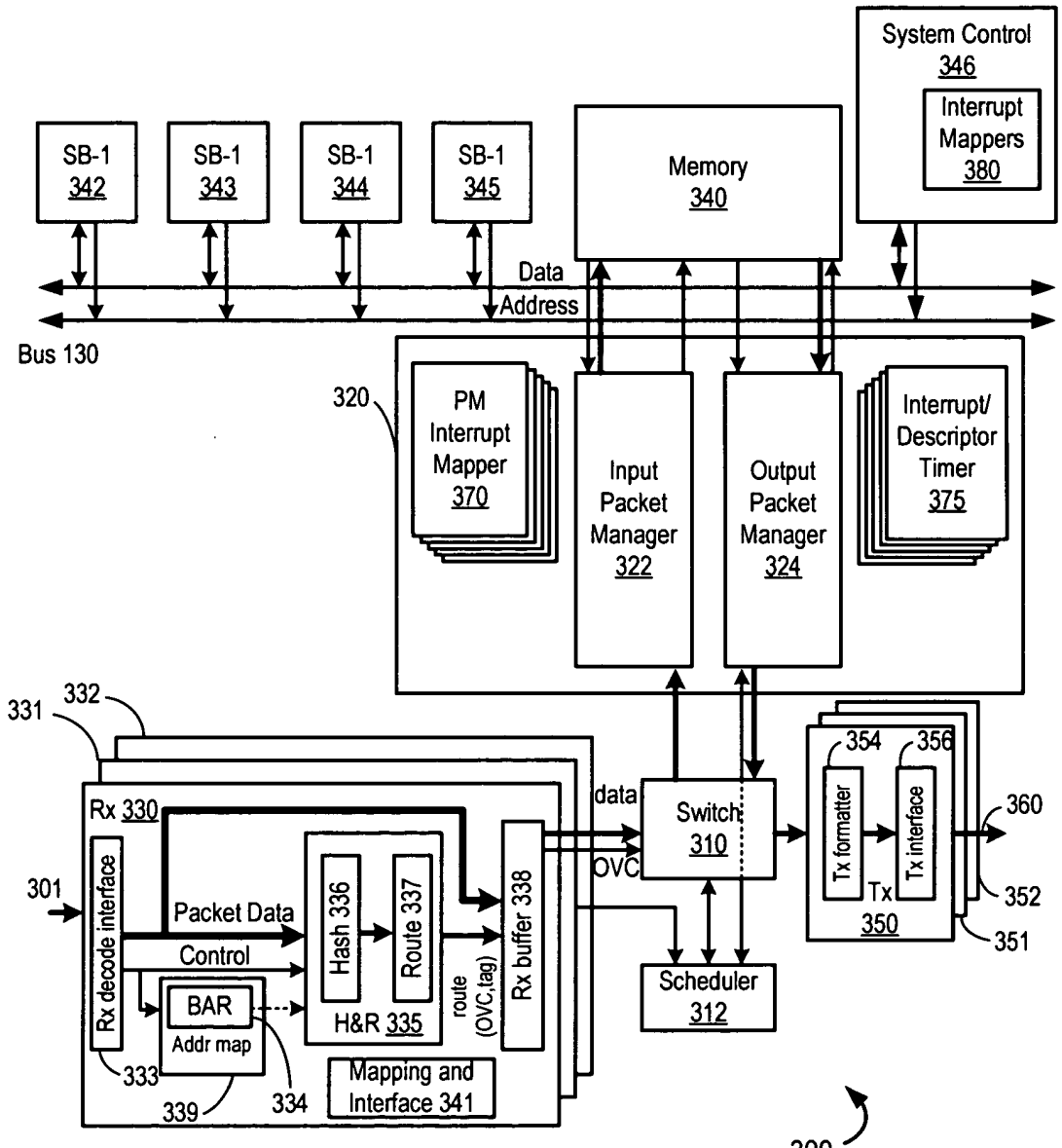

System Control
346
Interrupt
Mappers
380
SB-1
342
SB-1
343
SB-1
344
SB-1
345
Memory
340
Data
Address
Bus 130
320
PM
Interrupt
Mapper
370
Input
Packet
Manager
322
Output
Packet
Manager
324
Interrupt/
Descriptor
Timer
375
331
332
Rx 330
301
Rx decode interface
Packet Data
Control
BAR
Addr map
333
339
334
Hash 336
Route 337
H&R 335
route
(OVC,tag)
Rx buffer 338
Mapping and
Interface 341
data
OVC
Switch
310
Scheduler
312
354
356
Tx formatter
Tx interface
Tx
350
360
352
351
300

Figure 3

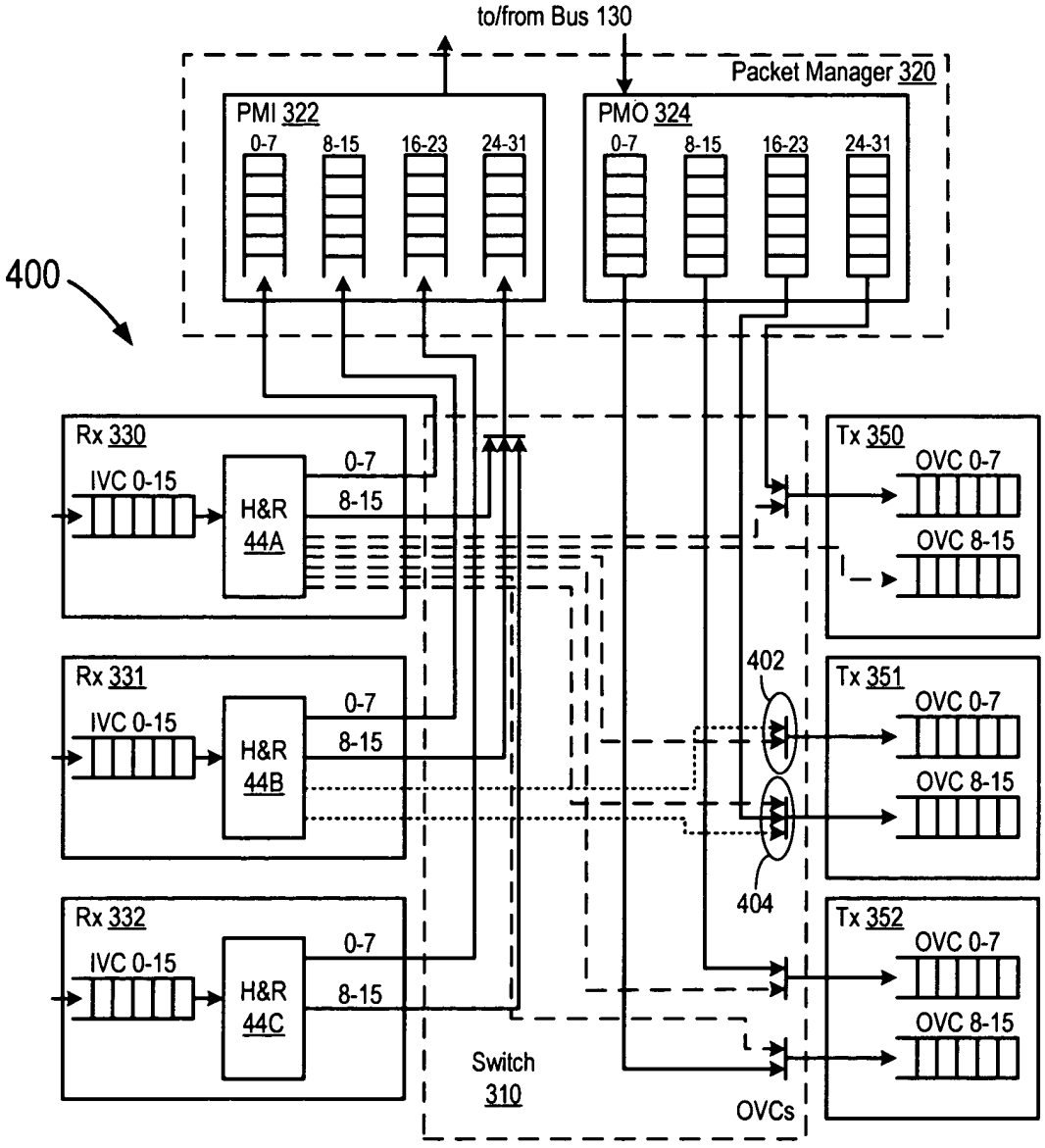

to/from Bus 130
Packet Manager 320
PMI 322
0-7
8-15
16-23
24-31
PMO 324
0-7
8-15
16-23
24-31
400
Rx 330
IVC 0-15
H&R
44A
0-7
8-15
Rx 331
IVC 0-15
H&R
44B
0-7
8-15
Rx 332
IVC 0-15
H&R
44C
0-7
8-15
Switch
310
Tx 350
OVC 0-7
OVC 8-15
Tx 351
OVC 0-7
OVC 8-15
Tx 352
OVC 0-7
OVC 8-15
402
404
OVCs

Figure 4

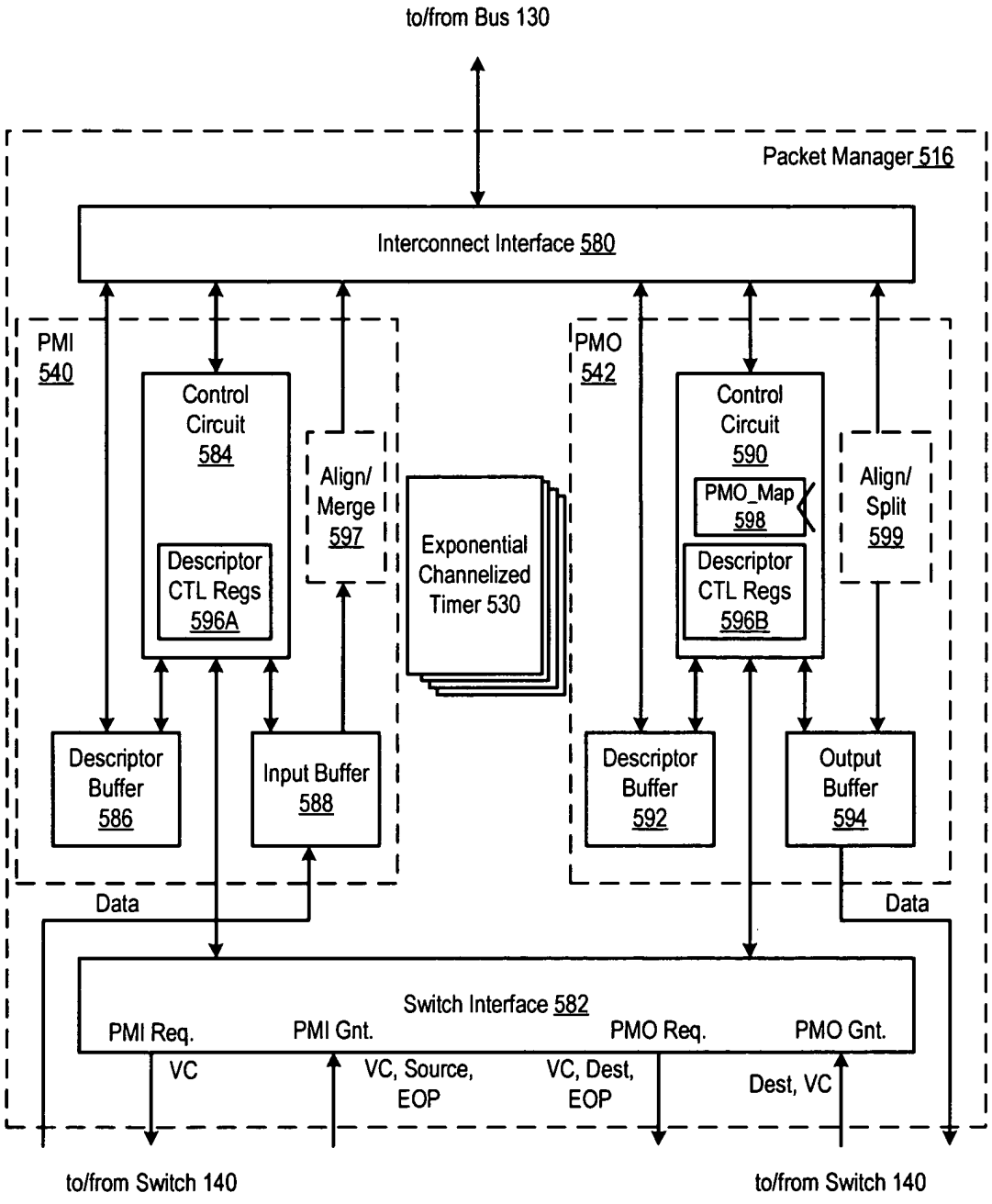
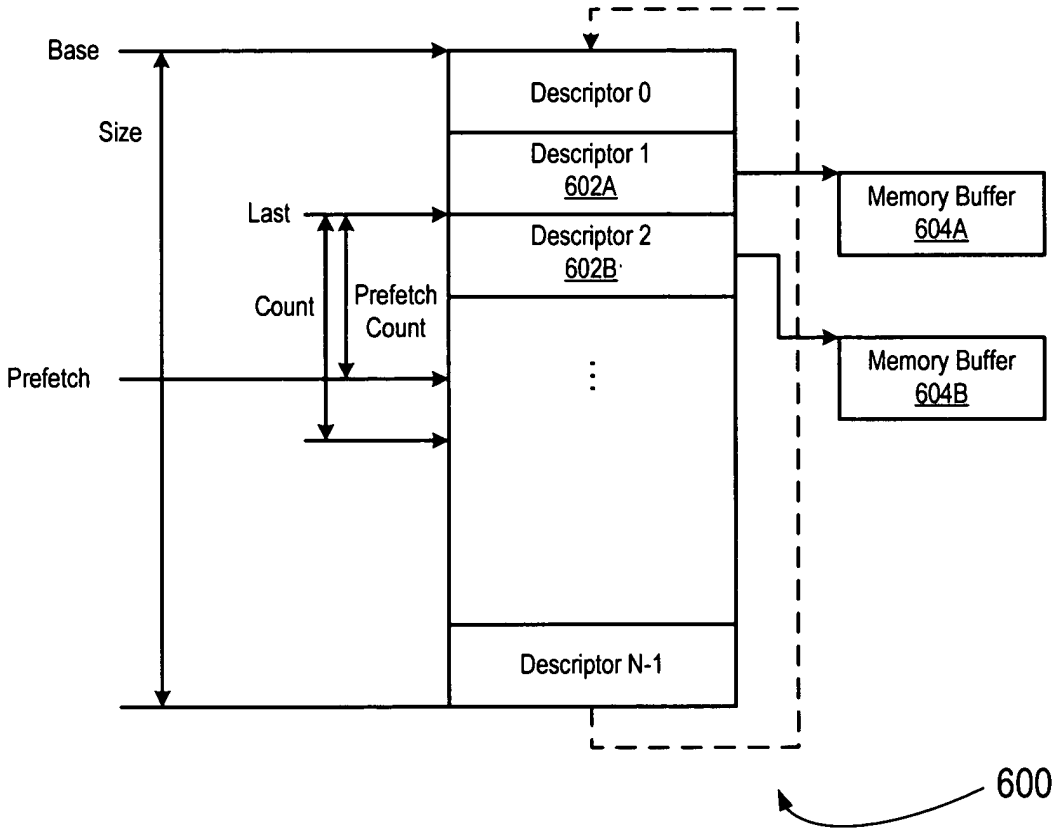

to/from Bus 130
Packet Manager 516
Interconnect Interface 580
PMI
540
Control
Circuit
584
Descriptor
CTL Regs
596A
Align/
Merge
597
Exponential
Channelized
Timer 530
PMO
542
Control
Circuit
590
PMO_Map
598
Descriptor
CTL Regs
596B
Align/
Split
599
Descriptor
Buffer
586
Input Buffer
588
Descriptor
Buffer
592
Output
Buffer
594
Data
Data
Switch Interface 582
PMI Req.
PMI Gnt.
PMO Req.
PMO Gnt.
VC
VC, Source,
EOP
VC, Dest,
EOP
Dest, VC
to/from Switch 140
to/from Switch 140

Figure 5


Base
Size
Last
Count
Prefetch Count
Prefetch
Descriptor 0
Descriptor 1
602A
Descriptor 2
602B
Descriptor N-1
Memory Buffer
604A
Memory Buffer
604B
600

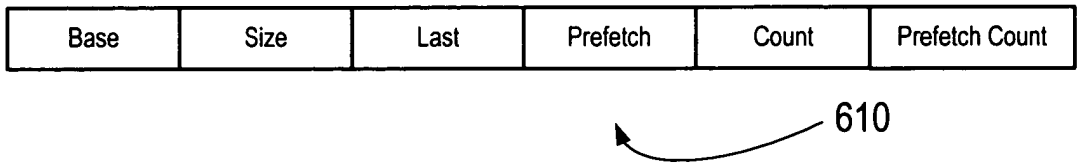

Base
Size
Last
Prefetch
Count
Prefetch Count
610

Figure 6

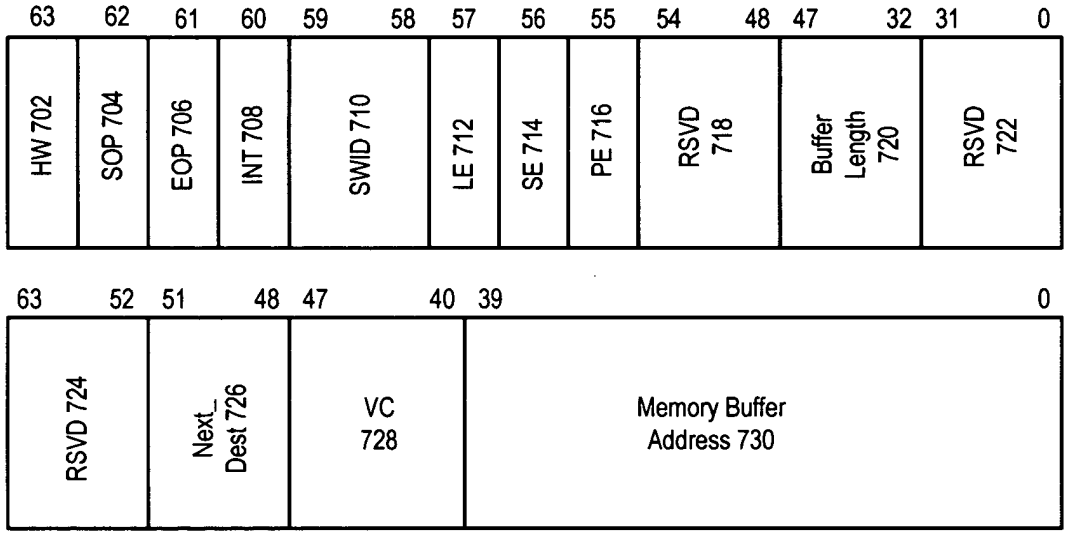

63
62
61
60
59
58
57
56
55
54
48
47
32
31
0
HW 702
SOP 704
EOP 706
INT 708
SWID 710
LE 712
SE 714
PE 716
RSVD 718
Buffer Length 720
RSVD 722
63
52
51
48
47
40
39
0
RSVD 724
Next_ Dest 726
VC 728
Memory Buffer Address 730
602

Figure 7

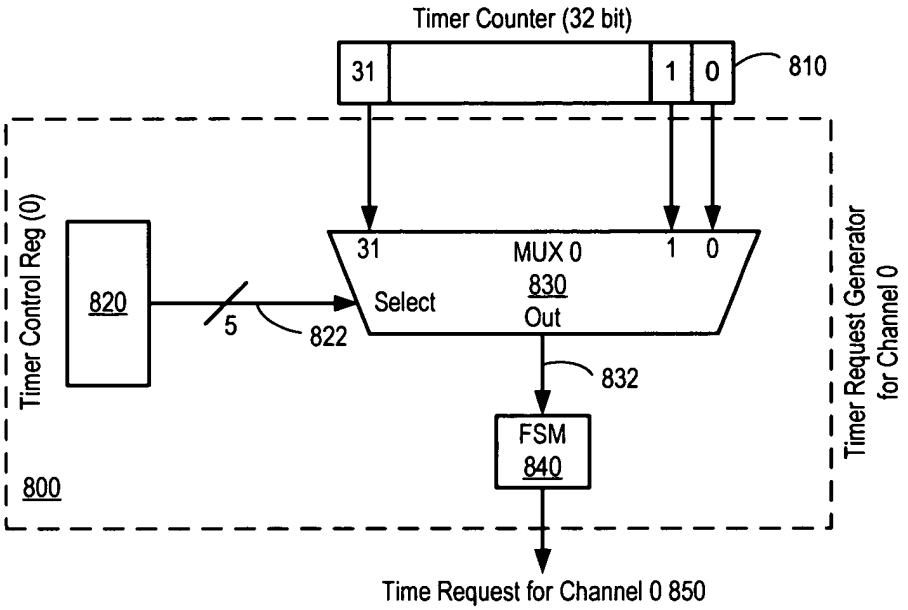


Figure 8

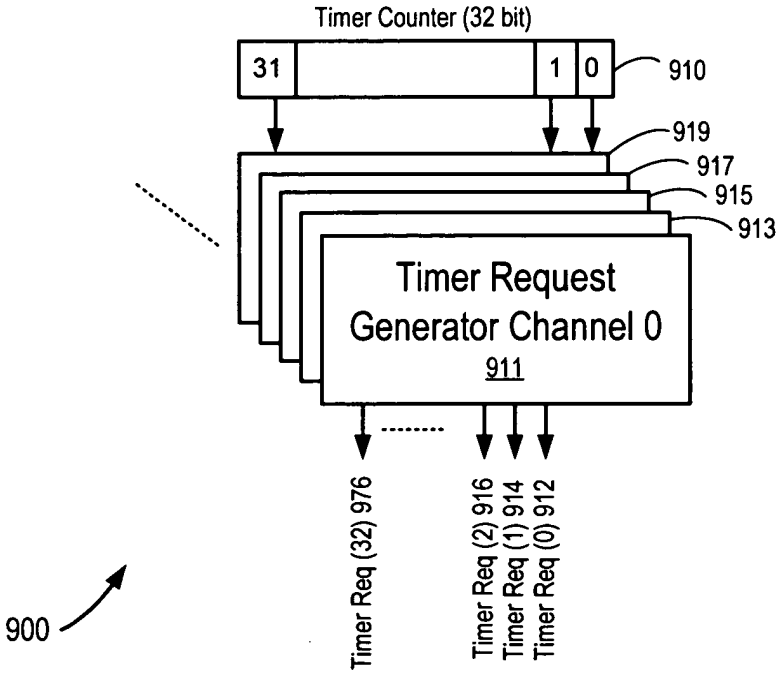


Figure 9

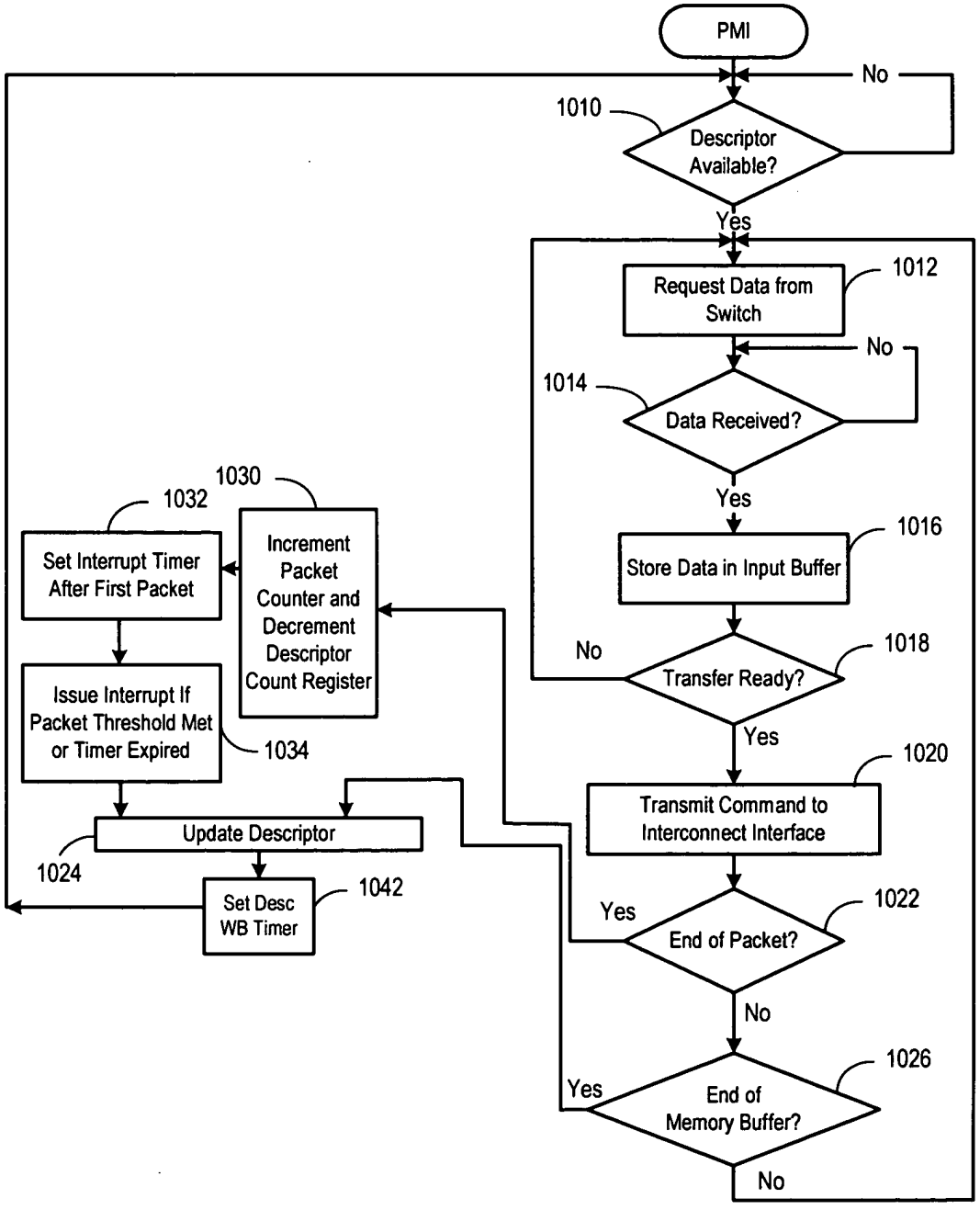

PMI
No
1010
Descriptor Available?
Yes
Request Data from Switch
1012
No
1014
Data Received?
Yes
1030
1032
Increment Packet Counter and Decrement Descriptor Count Register
Set Interrupt Timer After First Packet
Store Data in Input Buffer
1016
No
1018
Transfer Ready?
Issue Interrupt If Packet Threshold Met or Timer Expired
1034
Yes
1020
Transmit Command to Interconnect Interface
Update Descriptor
1024
Yes
1022
End of Packet?
Set Desc WB Timer
1042
No
1026
Yes
End of Memory Buffer?
No

Figure 10

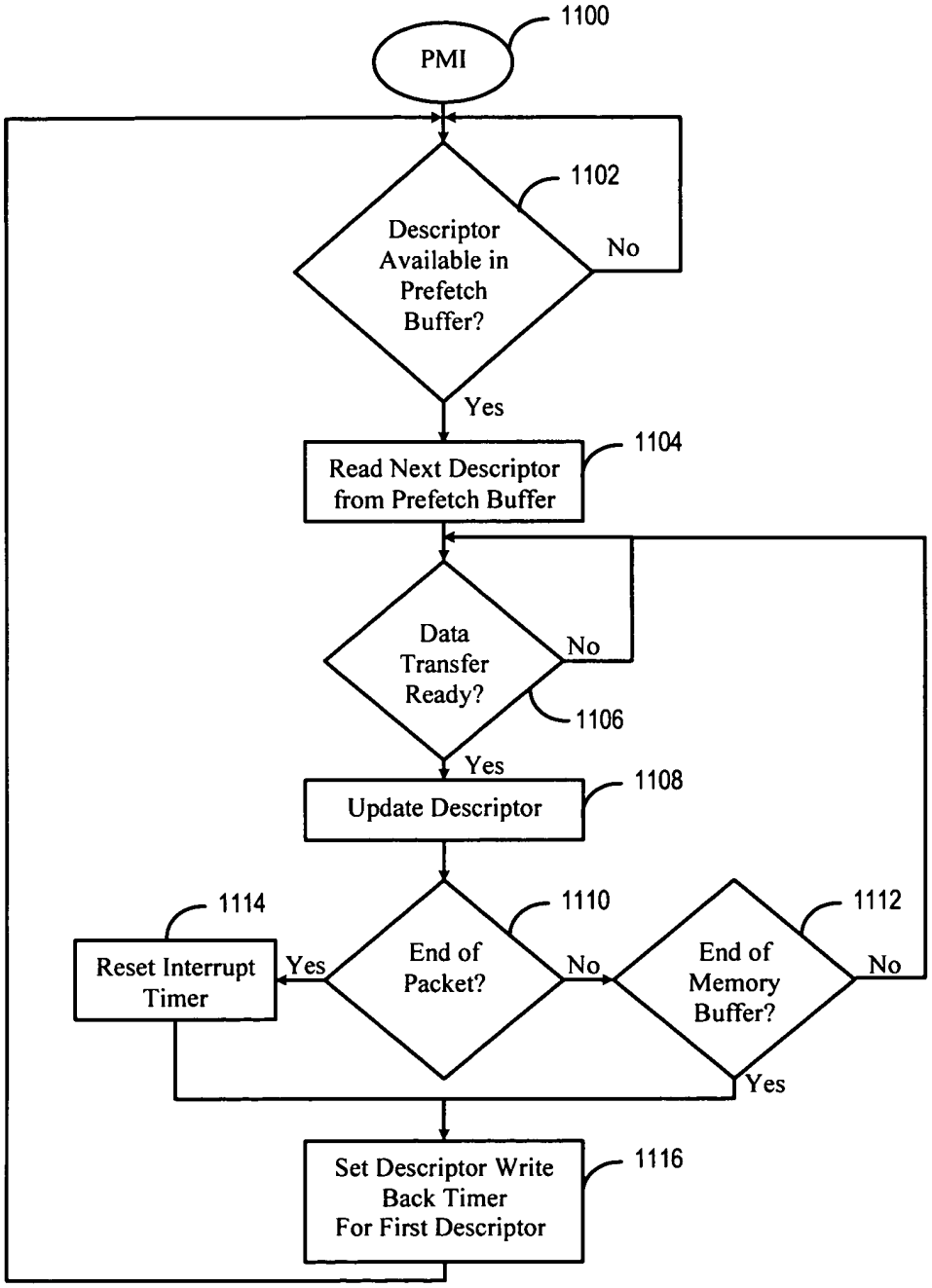

1100
PMI
1102
Descriptor Available in Prefetch Buffer?
No
Yes
1104
Read Next Descriptor from Prefetch Buffer
Data Transfer Ready?
No
1106
Yes
1108
Update Descriptor
1114
Reset Interrupt Timer
Yes
1110
End of Packet?
No
1112
End of Memory Buffer?
No
Yes
1116
Set Descriptor Write Back Timer For First Descriptor

Figure 11

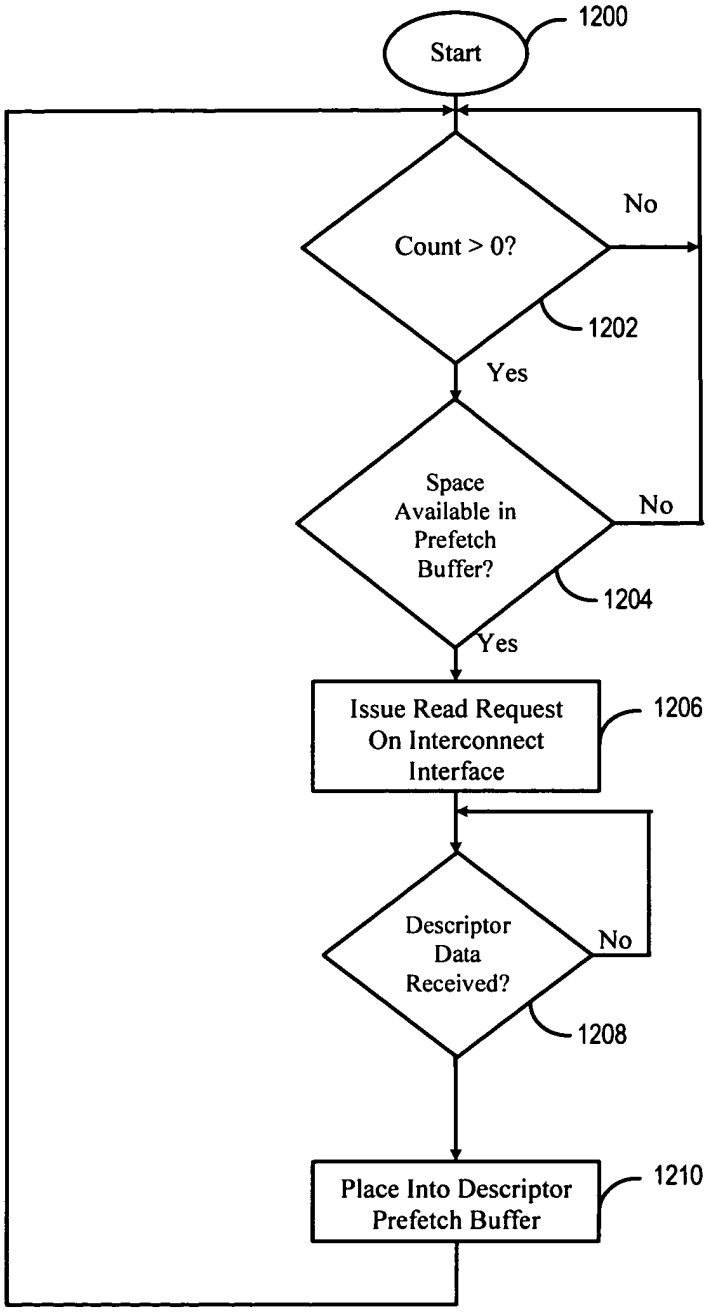

1200
Start
Count > 0?
No
1202
Yes
Space Available in Prefetch Buffer?
No
1204
Yes
Issue Read Request On Interconnect Interface
1206
Descriptor Data Received?
No
1208
Place Into Descriptor Prefetch Buffer
1210

Figure 12

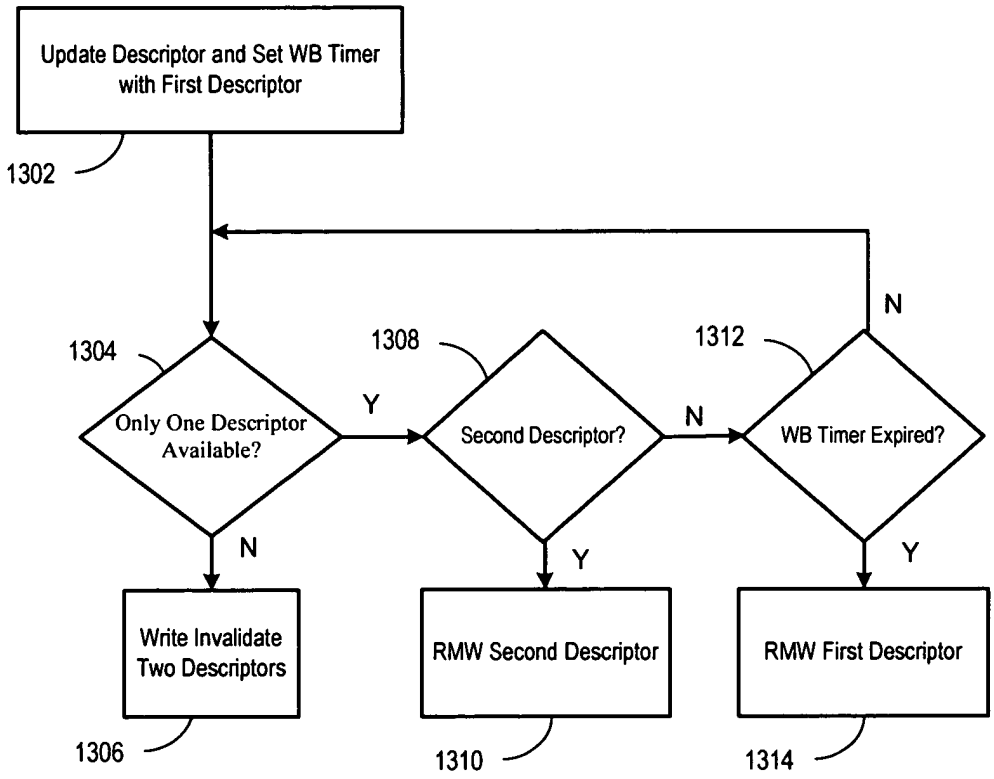

Update Descriptor and Set WB Timer with First Descriptor
1302
1304
Only One Descriptor Available?
Y
1308
Second Descriptor?
N
1312
WB Timer Expired?
N
N
Y
Y
Write Invalidate Two Descriptors
1306
RMW Second Descriptor
1310
RMW First Descriptor
1314

Figure 13